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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/017,198 | 12/18/2001 | Yuki Kondoh | HITA.0142 | 6344 |

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| EXAMINER | |
|---|---|
| COLEMAN, ERIC | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | |

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/017,198 | KONDOH ET AL. | |
| | Examiner | Art Unit | |
| | Eric Coleman | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12 and 13* is/are rejected.

7)☒ Claim(s) *11,14,15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6,8,10,12 are rejected under 35 U.S.C. 102(e) as being anticipated by O'Connor (patent No. 6,237,087).

3. O'Connor taught the invention as claimed including a data processing ("DP") system comprising:

a) An instruction fetching circuit for calculating a lower portion of an effective address for an instruction word (212) with a displacement (210), for replacing a value of the displacement in the instruction word according to the calculating result, and for storing the value in a storage circuit (252) (e.g., see figs. 2,3,4 and col. 4, lines 39-col. 6 line 49); and

b) The storage the circuit (252) for temporarily storing the instruction word, from which the stored instruction word is read at an instruction execution time wherein the effective address of the instruction word in the storage circuit is specified relative to a current value of a program counter address at the instruction execution time with the displacement, and wherein the processor utilizes the value stored in the storage circuit

as a lower portion of the effective address at the instruction execution time ) (e.g., see figs. 2,3,4, and col. 4, lines 39-col. 6 line 49).

4. As per claim 2, O'Connor taught the storage circuit that has additional areas each of which one-on-one corresponds to each the instruction word, and the storage storage circuit stores the calculating result in the additional storage areas (e.g., see col. 1, line 66-col. 3 line, 32).

5. As per claims 3,4, O'Connor taught the effective address is a branch target address (e.g., see col. 3, lines 49-65).

6. As per claims 5,10 O'Connor taught the storage circuit is a cache or buffer (e.g., see figs. 2,3,4 and col. 3, lines 49-65).

7. As to the further limitations of claim 6, O'Connor taught a storage circuit (discussed above), a decoder (320) for receiving the instruction word and for determining whether an effective address of the instruction word is specified as a PC relative displacement value (e.g., see figs. 3,4 and col. 5, line 6-22), and adder for adding of the PC relative displacement value and predetermined lower bits of the PC address, and for outputting the calculating result outputted from the adder as a portion of the effective address if the instruction word has the PC relative displacement value(e.g., see fig. 2 and col. 5, lines 12-55); and selector (326,344,332) for replacing the displacement value in the instruction word with the calculating result outputted from the adder and for outputting the replaced result to the storage circuit as a semi/ABS displacement value of the instruction word (or equivalent of semi/ABS displacement

value), if the instruction has the PC relative displacement value (e.g., see col. 5, lines 6-55).

8. As per claim 8, O'Connor taught the storage circuit including and area for storing a carry bit from the adder corresponding to the instruction word (e.g., see fig. 2 and col. 5, lines 39-55 and col. 4, lines 60-65).

9. As to the limitations of claim 12, O'Connor taught a method for converting a first instruction word with a PC relative displacement value into a second instruction word with a semi/ABS displacement value (or displacement equivalent to a semi/ABS displacement value) comprising; calculating a semi/ABS or equivalent displacement value by adding predetermined lower bits of a PC address and the PC relative displacement value; replacing the PC relative displacement value in the first instruction word with the calculating result; and storing the second instruction word with the semiABS or equivalent displacement value in a storage circuit, whereby the semi semiABS or equivalent displacement value stored in the storage circuit is then immediately used as a portion of an effective address at the instruction execution time (e.g., see figs. 2,3,4, and col. 4, lines 39-col. 6 line 49).

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 7,9,13 rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor.

O'Connor taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) An instruction fetching circuit for calculating a lower portion of an effective address for an instruction word (212) with a displacement (210), for replacing a value of the displacement in the instruction word according to the calculating result, and for storing the value in a storage circuit (252) (e.g., see figs. 2,3,4 and col. 4, lines 39-col. 6 line 49); and

b) The storage the circuit (252) for temporarily storing the instruction word, from which the stored instruction word is read at an instruction execution time wherein the effective address of the instruction word in the storage circuit is specified relative to a current value of a program counter address at the instruction execution time with the displacement, and wherein the processor utilizes the value stored in the storage circuit as a lower portion of the effective address at the instruction execution time ) (e.g., see figs. 2,3,4, and col. 4, lines 39-col. 6 line 49).

12. As per claim 2, O'Connor taught the storage circuit that has additional areas each of which one-on-one corresponds to each the instruction word, and the storage storage circuit stores the calculating result in the additional storage areas (e.g., see col. 1, line 66-col. 3 line, 32).

13. As per claims 3,4, O'Connor taught the effective address is a branch target address (e.g., see col. 3, lines 49-65).

14. As per claims 5,10 O'Connor taught the storage circuit is a cache or buffer (e.g., see figs. 2,3,4 and col. 3, lines 49-65).

15. As to the further limitations of claim 6, O'Connor taught a storage circuit (discussed above), a decoder (320) for receiving the instruction word and for determining whether an effective address of the instruction word is specified as a PC relative displacement value (e.g., see figs. 3,4 and col. 5, line 6-22), and adder for adding of the PC relative displacement value and predetermined lower bits of the PC address, and for outputting the calculating result outputted from the adder as a portion of the effective address if the instruction word has the PC relative displacement value(e.g., see fig. 2 and col. 5, lines 12-55); and selector (326,344,332) for replacing the displacement value in the instruction word with the calculating result outputted from the adder and for outputting the replaced result to the storage circuit as a semi/ABS displacement value of the instruction word (or equivalent of semi/ABS displacement value), if the instruction has the PC relative displacement value (e.g., see col. 5, lines 6-55).

16. As per claim 8, O'Connor taught the storage circuit including and area for storing a carry bit from the adder corresponding to the instruction word (e.g., see fig. 2 and col. 5, lines 39-55).

17. As to the limitations of claim 12, O'Connor taught a method for converting a first instruction word with a PC relative displacement value into a second instruction word with a semi/ABS displacement value (or displacement equivalent to a semi/ABS displacement value) comprising; calculating a semi/ABS or equivalent displacement

value by adding predetermined lower bits of a PC address and the PC relative displacement value; replacing the PC relative displacement value in the first instruction word with the calculating result; and storing the second instruction word with the semiABS or equivalent displacement value in a storage circuit, whereby the semi semiABS or equivalent displacement value stored in the storage circuit is then immediately used as a portion of an effective address at the instruction execution time (e.g., see figs. 2,3,4, and col. 4, lines 39-col. 6 line 49).

18. As per claims 7,9,13, O'Connor taught that in cases where the displacement size was smaller the number of bits needed to address the cache, two options existed either pre-compute enough bits to address the cache and add additional storage to the cache to make room for these extra bits, or to use only one bit of additional (storage for the carry) and have an incrementer that used this carry to compute the remaining bits needed to access the cache (e.g. see col. 6, lines 9-18). Therefore one of ordinary skill would have been motivated to sign extend the displacement in the embodiment when the carry was stored and an incrementer was used to compute the additional bits for computing the effective address. This would allow the system to indicate, by the number of extended by sign bits, how many bits would be added to the displacement for calculation of the effective address. This would have provided for efficiently providing the proper length effective address such as by masking or multiplexing the bits of a portion of the instruction using the extended instruction bits. This would have been necessary in the case where the displacement did not contain enough bits to address the cache.

### *Allowable Subject Matter*

Claims 11,14, and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Amendment*

19. Applicant's arguments with respect to claims 1-10,12,13 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER